This listing of claims will replace all prior versions, and listings, of claims in the application:

The Status of the Claims

1. (Currently Amended) A method of forming a gate in a semiconductor device, the method comprising:

forming on a semiconductor substrate a gate oxide layer and then forming on the semiconductor substrate a sacrificial layer;

selectively etching the sacrificial layer to form a sidewall opening;

forming a polycrystalline silicon layer on an area of the gate oxide layer exposed through the sidewall opening and on the sacrificial layer;

performing anisotropic etching of the polycrystalline silicon layer such that sidewall gates are formed by remaining portions of the polycrystalline silicon layer on sidewalls of the sidewall opening, a width of the sidewall gates corresponding to a desired width of a gate; and

removing the sacrificial layer.

2. (Original) A method as defined by claim 1, wherein the sacrificial layer comprises a nitride layer.

3. (Original) A method as defined by of claim 2, wherein the nitride layer is removed using a wet etching process.

4. (Original) A method as defined by claim 1, wherein the sacrificial layer is removed using a wet etching process.

5. (Original) A method as defined by claim 1, wherein anisotropic etching of the polycrystalline layer comprises an etch-back process.

6. (Original) A method as defined by claim 1, wherein the width of the sidewall gates is determined by a thickness of the sacrificial layer.

7. (Original) A method as defined by claim 1, wherein the width of the sidewall opening formed by selectively etching the sacrificial layer corresponds to a width from one gate to an adjacent gate.

8. (Original) A method as defined by claim 7, wherein the sacrificial layer comprises a nitride layer.

9. (Original) A method as defined by claim 8, wherein the nitride layer is removed using a wet etching process.

10. (Original) A method as defined by claim 7, wherein the sacrificial layer is removed using a wet etching process.

11. (Original) A method as defined by claim 7, wherein anisotropic etching of the polycrystalline layer is an etch-back process.

12. (Original) A method as defined by claim 7, wherein the width of the sidewall gates is determined by a thickness of the sacrificial layer.

13. (New) A method as defined by claim 1, wherein the sidewall gates are divided by a trench.